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# Reduced Switch Count Topology for a Series Parallel Switched Multilevel Inverter

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**Abstract**

*The paper brings out a new three phase series parallel switched cascaded multilevel inverter (SPSWCMLI) with a reduced number of power switches in the path of the current. It allows a series parallel path for the flow of current and engages a change in the modulation index to extract a variable output voltage. The approach pronounces the advantages of a modulation technique for the inverted sine carrier pulse width modulation (ISCPWM) to confirm removal of the higher frequency components of the output voltage. The modulating mechanism also causes the fundamental component of both the output line and the phase voltage to increase significantly. Using comparatively smaller number of carriers in the process of producing the switching pulses helps to increase the range of output voltage. The intriguing merits of the phase disposition (PD) over the other modulation schemes allow for an almost sinusoidal voltage to be reached. The hardware-based investigative analysis aims to verify the simulated findings and highlight the importance of the proposed reduced switch count multilevel inverter (MLI) in terms of lowering the capital cost and enhancement in the quality of the output voltage.*

**Keywords:** *Multilevel inverter, total harmonic distortion, inverted sine carrier pulse width modulation, phase disposition.*

## INTRODUCTION

Multilevel power conversion seems to be focusing on gathering strength for use in high-power medium-voltage applications that include a variety of applications. The MLI produce stepped output voltage waveform by proper arrangements of semiconductor switches and either isolated or non-isolated dc voltage sources. The rise in the number of output voltage levels helps to follow a sinusoidal pattern and to minimize the distortion [1]. The MLIs try to diminish the stress on the switching device by following a reduced path for the current and the presence of lower-level voltage sources through its operational flexibility.

The introduction of different MLI topologies designs a new direction to be used in high voltage and high power applications. Recent MLI applications include induction machine drives , active rectifiers, laminators, conveyors, pumps, blowers, and compressors[2]. While the classical topologies of the multilevel voltage source inverter include diode-clamped, flying capacitor and cascaded H-bridge structures continue to meet the application requirements, the count of devices is still substantially high with the increase in voltage levels.

A new topology for the MLI was introduced to generate higher voltage levels at the inverter output with reduced switching devices. A hybrid modulation scheme was used to minimize the harmonic distortion[3]. The conventional and concurrent MLI structures was compared with the performance of the proposed topology by simulation results.

A new single-phase cascaded multi-level inverter (CMLI) topology was proposed to make optimized use of dc source and reduced switch count [4]. Simulations in MATLAB / Simulink have tested the proposed design for its feasibility and results was confirmed by experimental set-up of a single-phase prototype model.

A new MLI was proposed to provide an nearly sinusoidal variable voltage. The formulation was

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strengthened by the usage of a new PWM strategy to require rise in the fundamental component of the output voltage and a corresponding decrease in its total harmonic distortion (THD) [5]. The results of the MATLAB-based simulation were tested using a prototype model. For firing the power switches in the MLI an ISCPWM method was applied. The ISCPWM based PD was seen as offering a higher fundamental voltage compared to the triangular based pulse width modulation (PWM) generation for different levels obtained from the identical topology [6].

A multicarrier pulse width modulation (MCPWM) method was outlined for controlling the performance of a three level inverter. It was designed constant carrier frequency not synchronized fundamental strategy frequency [7]. The results from the MATLAB simulation was shown to yield a good performance for the MCPWM compare to the other methods.

The trend revolves around the usage of reduced switch count configurations that perceive paths for the flow of current from a smaller number of power sources and still allow achieving the desired number of levels. However it envisages the use of suitable PWM strategies to attain at a quality output voltage. Developments in PWM techniques require a space in which to adapt to the latest topologies and open up avenues for its practical implementation.

**PROBLEM FORMULATION**

The focus is on exploring the use of an ISCPWM strategy to produce a variable voltage from a SPSWCMLI . The theory revolves around the requirement of increasing the fundamental component and reducing the THD of the output voltage. It evaluates the performance of a ISCPWM strategy with much lower number of carriers for providing a variable voltage . It requires the use of the field programmable gate array ( FPGA) based prototype to substantiate the results of the simulation and erudite the advantages of the formulation.

**PROPOSED METHODOLOGY**

The primary effort concerns the creation of a new three phase SPSWCMLI topology with the number of cells according to the number of levels to meet the power requirements of the RL load connected across the proposed MLI 's outer H-bridge. It falls within the cascaded MLI group, and ventures to minimize the number of switches in the current flow direction. The structure's generalized existence demonstrates its flexible ability to achieve the desired number of output levels by increasing the number of cells. The fundamental emphasis extends towards deriving nearly sinusoidal output voltage with least number of active devices and providing lower THD rates across the operating range.

The generalized structure seen in Fig.1 integrates modular cells with a bidirectional switch across each of them together with a H-bridge in each phase to offer the specified power at the prescribed voltage for the RL load. A dc voltage source, two bidirectional and one unidirectional switch in the central limb forms each cell. The dc voltages in the cells pick on equal magnitudes for the three phases to realize a symmetrical output voltage waveform.

The letters ($S_{a1}$…. $S_{a(4k)}$), ($S_{b1}$…. $S_{b(4k)}$) and ($S_{c1}$…. $S_{c(4k)}$) represent the active devices in each phase respectively and the unidirectional switches ($S_1$ - $S_4$) , ($S_5$ - $S_8$) and ($S_9$ - $S_{12}$) constitute the H-bridge inverters and k stands for the number of cells in the topology.

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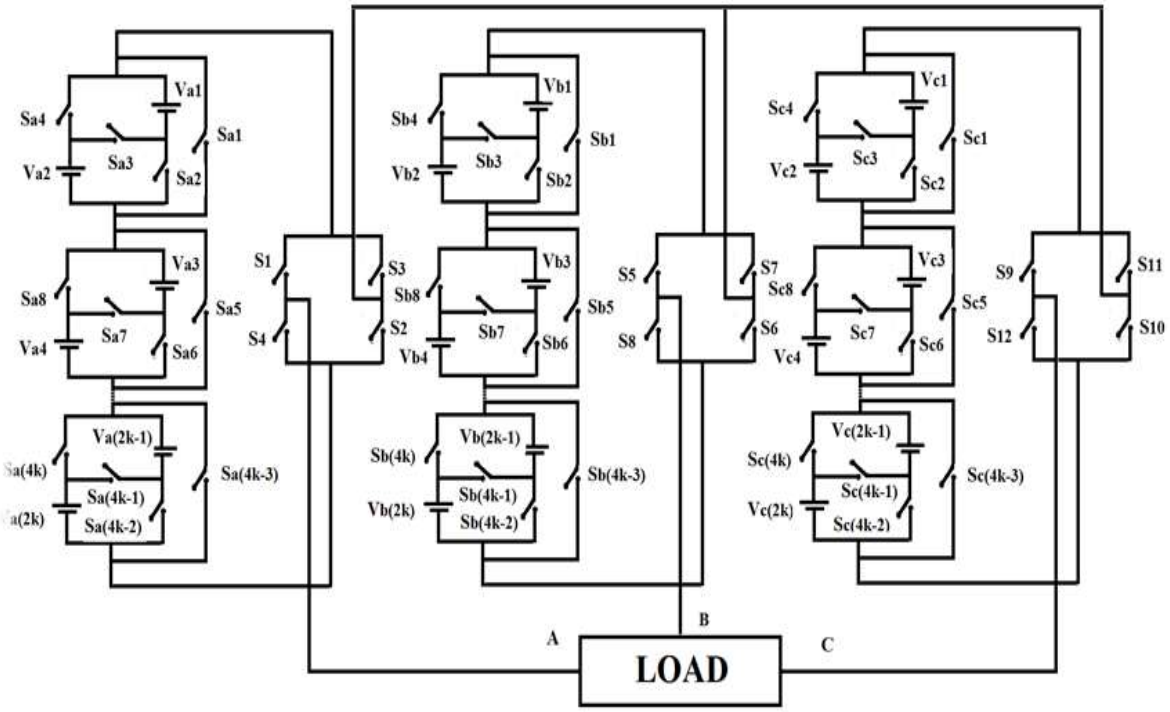


Fig. 1 Elementary structure of proposed three phase SPSWCMLI

**OPERATING MODES**

The section of the power module of the proposed nine-level MLI relevant to Phase A shown in Fig.2(a) includes the bidirectional switches $S_{a1}$, $S_{a2}$, $S_{a4}$, $S_{a5}$, $S_{a6}$, $S_{a8}$ and the unidirectional switches $S_{a3}$, $S_{a7}$, $S_1$ , $S_2$, $S_3$, $S_4$ to allow the current to flow in Phase A. The usage of bidirectional devices allows the path of flowing current in the cell to be prevented. Similarly, in the other two phases, the switches $S_{b1}$, $S_{b2}$, $S_{b4}$, $S_{b5}$, $S_{b6}$, $S_{b8}$ and $S_{b3}$, $S_{b7}$, $S_5$, $S_6$ , $S_7$, $S_8$ and $S_{c1}$, $S_{c2}$, $S_{c4}$, $S_{c5}$, $S_{c6}$, $S_{c8}$ and $S_{c3}$, $S_{c7}$, $S_9$, $S_{10}$, $S_{11}$, $S_{12}$ carry the power. The diagrams shown in Figs.2(b) and 2(c) illustrate the operating modes for generating $+4V_{DC}$ and $-4V_{DC}$ for the Phase A output for the nine level MLI, and the entries in Table 1 refer to the switches involved in each operating mode for the first phase of the three phase MLI.

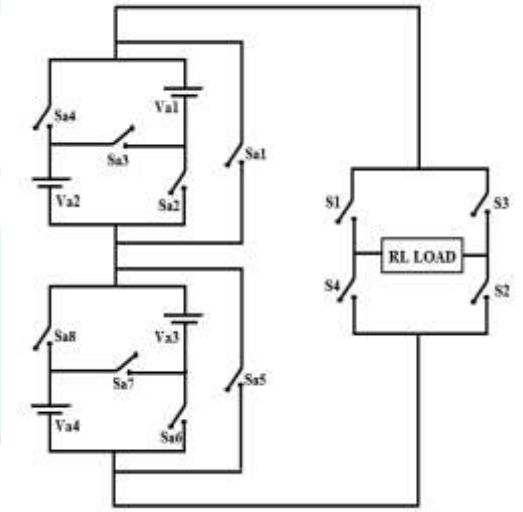


Fig 2 (a) Topology for producing nine-level output for phase A (b) $+4V_{DC}$ output and (c) $-4V_{DC}$ output

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Table 1

Switching Sequence of nine level output for Phase A

| Levels of Output Voltage | Conduction of Switches | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $S_{a1}$ | $S_{a2}$ | $S_{a3}$ | $S_{a4}$ | $S_{a5}$ | $S_{a6}$ | $S_{a7}$ | $S_{a8}$ | $S_1$ | $S_2$ | $S_3$ | $S_4$ |
| $+V_{DC}$ | √ | | | | | √ | | √ | √ | √ | | |
| $+2\ V_{DC}$ | √ | | | | | | √ | | √ | √ | | |
| $+3\ V_{DC}$ | | √ | | √ | | | √ | | √ | √ | | |
| $+4\ V_{DC}$ | | | √ | | | | √ | | √ | √ | | |
| $0\ V_{DC}$ | √ | | | | √ | | | | √ | | √ | |
| $-\ V_{DC}$ | √ | | | | | √ | | √ | | | √ | √ |
| $-2\ V_{DC}$ | √ | | | | | | √ | | | | √ | √ |
| $-\ 3\ V_{DC}$ | | √ | | √ | | | √ | | | | √ | √ |
| $-\ 4\ V_{DC}$ | | | √ | | | | √ | | | | √ | √ |

Fig.3 compares the number of active power switches and dc sources required to obtain increasing levels of output voltage per phase for both the proposed SPSWCMLI and the cascaded H-bridge multilevel inverter (CHBMLI) to determine the reduction in the count of switch and outlines the advantages of the proposed MLI topology . It follows that the number of active switches for increasing levels of per phase output voltage in the SPSWCMLI increases in accordance with the relation 4k+4 and 8k for the CHBMLI. Owing to the fact that the SPSWCMLI topology requires a least number of switches, it benefits from a reduced number of associated gate drivers and ends up with a relatively lower capital cost.

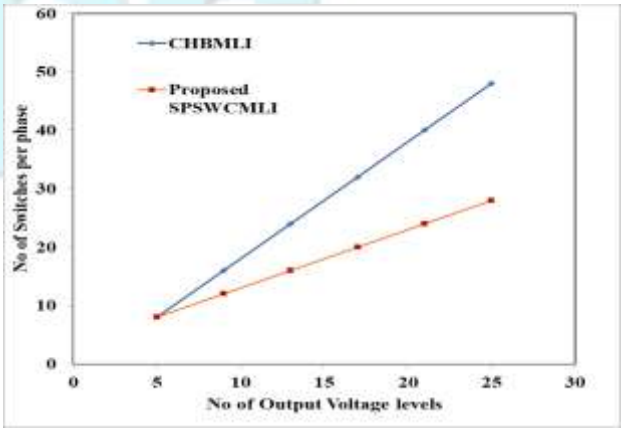


Fig. 3 Comparison of SPSWCMLI and CHBMLI

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**MODULATION STRATEGY**

Modulation strategies associated to the switching activity in MLIs echo to establish revival in the sense that it promotes a dissimilar perspective for its use. It refers to the way information is conveyed through a train of pulses and allows the information to be encoded in the width of pulses. The central theme prompts control of the output voltage of the inverter and serves to reduce its harmonic content. In addition to introducing changes in the shape of the reference sine wave, the variation in the carrier's amplitude and frequency appear to be the promising avenues for realizing enhancements in the output 's spectral quality.

Among the MCPWM methods that include phase disposition, alternative phase opposition arrangement and carrier polarity variation suitable for the operation of MLIs, the PD augurs to imbibe a significant portion of the harmonic energy within the main carrier wave region to extract significant harmonic performance over the other techniques[8]. The operation of an MLI largely depends on the effectiveness of the PWM scheme in being able to give an improvement in its performance. The influence of the nature of the carrier wave admonishes the ability to usurp a fresh scope for rearranging the higher frequency components of the output voltage.

The power converters feed a facility with the available switching devices to attain the specified voltage, and incorporate mechanisms to improve the output waveforms. The mechanism allows the triangular carrier to be replaced by an inverted sine wave so that a higher fundamental component and correspondingly a lower THD for the output voltage can be repealed. The substantial increase in THD over the lower range of modulation indices pronounces low-speed motor drive operation. The ISCPWM features the sinusoidal reference intersection and an inverted high frequency sine carrier to optimize output voltage over a choice of modulation index.

The increase of the fundamental amplitude in the sinusoidal pulse-width modulation becomes possible only in the over modulation region . However it inserts harmonics of lower order and distorts the non-linear relationship between the fundamental component and the modulation index. The alignment of the reference and carrier wave as shown in Figs.4 (a)and 4(b) for the PD-based MCPWM and ISCPWM relates to the PWM process for the Phase A switches, and the same procedure for the other two phases. The combinational circuits operate to include the superimposition of the inverted sine carrier wave with the sinusoidal reference in Fig. 5 and derive the PWM pulses for the power devices in the proposed MLI for phase A.

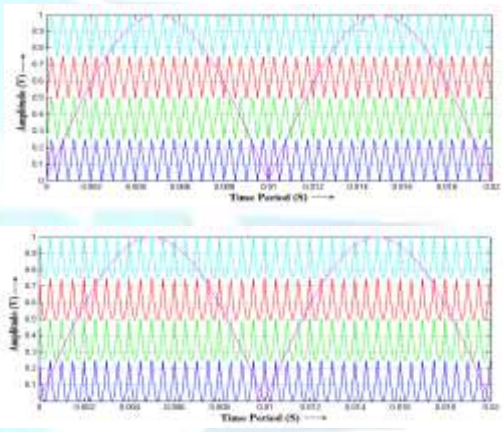

Figure 4 Reference and Carrier arrangement for Phase A using (a) PD MCPWM and (b) PD ISCPWM

SIMULATION RESULTS

The emphasis is on acquiring a sinusoidal variable voltage to generate 415 volts, which is three phase output according to the specific load requirements. It attempts to investigate the performance of the ISCPWM strategy on the new three-phase SPSWCMLI supported with the same 85 volts magnitudes for the rectified dc voltage sources in both cells through the MATLAB / Simulink platform to provide a nine-level output for the RL load. The output phase and line voltage waveforms and their respective THD spectra shown in Figs 6 through 9 corresponding to phase A and phase current waveform at a modulation index of 1 and a resistive-inductive load of 150 ohms and 100 mH respectively obtained using MCPWM and ISCPWM with a carrier frequency of 2 KHz to obtain the benefits of both the new topology and ISCPWM scheme . The bar and line sketches in

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Figs.10(a) and 10(b) establish the capability of the ISCPWM to accrue a higher for the phase A voltage. The Table. 2 shows the THD indices for the line voltage over the range of modulation indices and forges the fact that the ISCPWM accrues the ability to eliminate the higher frequency components of the output voltage more effectively than the MCPWM.

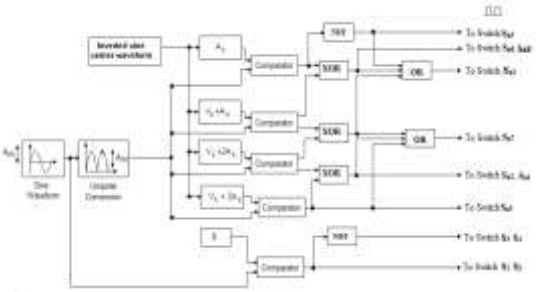


Figure 5 Generation of gating pulses using PD ISCPWM for Phase A

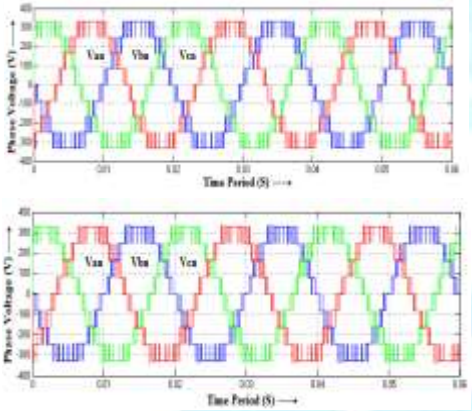



Figure 6 Waveform for Phase voltage using (a) PD MCPWM and (b) PD ISCPWM

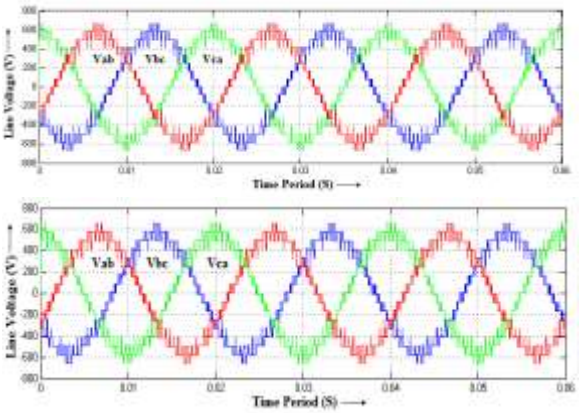



Figure 7 Waveform for Line voltage using (a) PD MCPWM and (b) PD ISCPWM

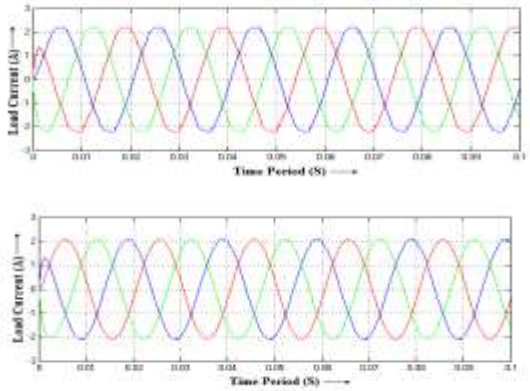
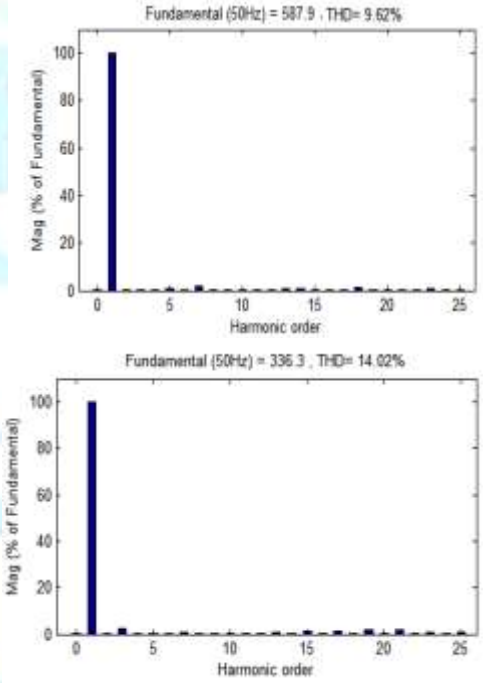



Figure 8 Waveform for Phase current using (a) PD MCPWM and (b)PD ISCPWM



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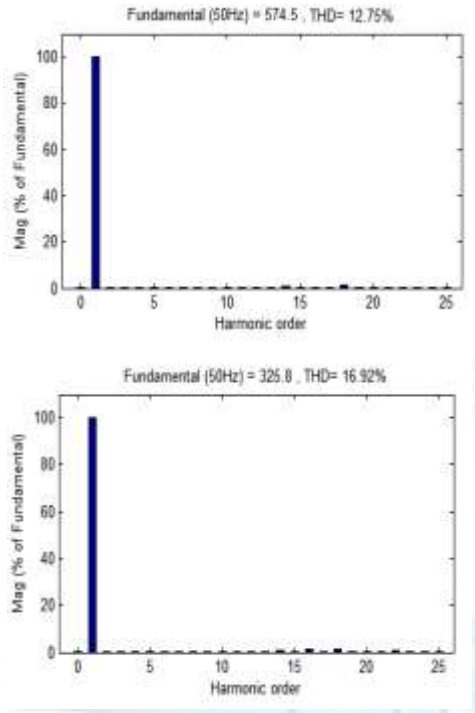


Figure 9 Spectrum for Phase voltage (Va) using (a) PD MCPWM, (b)PD ISCPWM, Line voltage (Vab) using (c) PD MCPWM and (d) PD ISCPWM

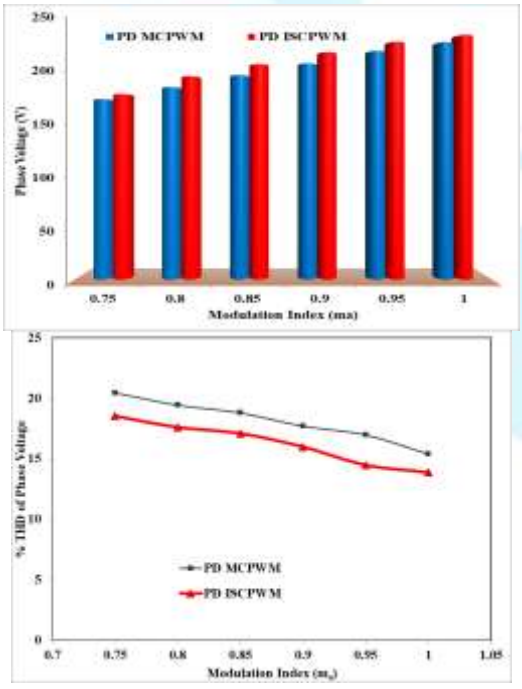


Figure 10 Variation of Modulation Index Vs (a) Phase Voltage (Va) (b) %THD of Phase Voltage (Va)

Table 2

Comparison of line voltage and % THD

| Modulation Index ($m_a$) | Line Voltage (V) | | | |
|---|---|---|---|---|
| | PD MCPWM | | PD ISCPWM | |
| | $V_{ab}$ | % THD | $V_{ab}$ | % THD |
| 1 | 404.6 | 12.75 | 415.1 | 9.62 |
| 0.95 | 386.8 | 14.16 | 404.5 | 10.82 |
| 0.9 | 364.9 | 15.03 | 383.1 | 12.02 |
| 0.85 | 344.1 | 15.97 | 364.8 | 12.81 |
| 0.8 | 325.4 | 16.61 | 342.7 | 13.94 |
| 0.75 | 303.5 | 17.97 | 312.1 | 14.89 |

HARDWARE IMPLEMENTATION

The procedure extends to construct the new three-phase SPSWCMLI with Insulated Gate Bipolar Transistor Power Devices (IRG4BC20UPBF-Unidirectional Device, FIO 50-12BD-Bidirectional Device) and DC voltage sources of the same ratings used in simulation. The photograph in Fig.11 shows the experimental prototype used to test the efficiency of the MLI and ISCPWM strategy being proposed.

The FPGA originates from an integrated circuit and can be modified to suit particular applications. It comprises an array of reprogrammable logic blocks and a hierarchy of reconfigurable interconnections that wire together the blocks. The most popular architecture in FPGA consists of several I/O pads and the same width of routing channels. The commonly defined FPGA design using a language of the hardware description develops by programming to realize a variety of applications.

The Xilinx offers the widest line-up of FPGAs offering advance features, low power and high performance for any design type. The flow chart in Fig. 12 explains the process for formation of the

pulses for Phase A using ISCPWM approach seen in Fig. 13 through the use of Xilinx XC3SD1800A-FG676-4 Spartan 3A DSP FPGA board. The output phase and the line voltage waveforms along with Phase A voltage and its current together with the harmonic spectrum seen in Figs. 14 to 16 are closely linked to the simulated results and help to translate the realities of the ISCPWM approach. It brings out the ISCPWM 's superiority over the MCPWM scheme via better spectral quality.

Figure.11 Experimental model of the three phase SPSWCMLI

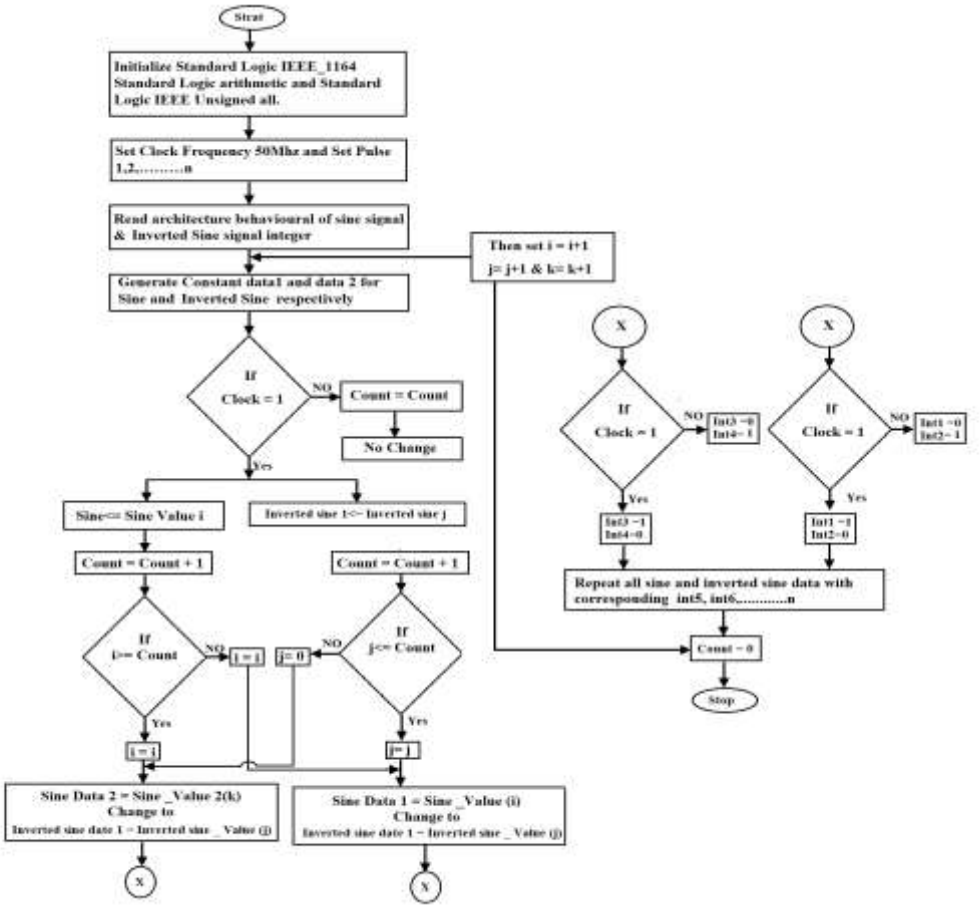


Figure 12 Generation of gating pulses using PD ISCPWM

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Figure 13 Switching pulses for Phase A using PD ISCPWM (a) Cell 1 (b) Cell 2 (c) H-Bridge

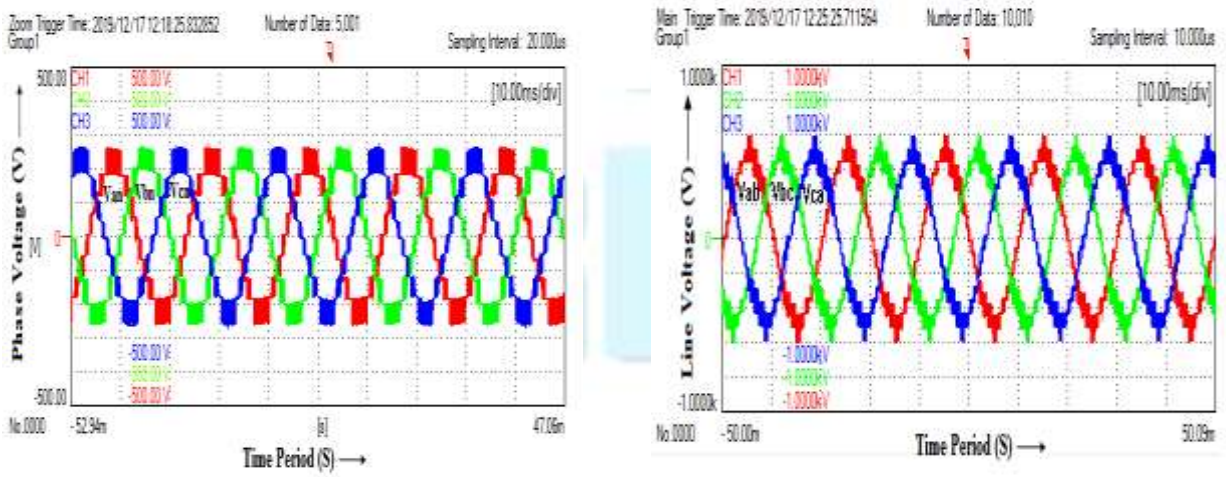


Figure 14 Waveform using PD ISCPWM for (a) Phase voltage and (b) Line voltage

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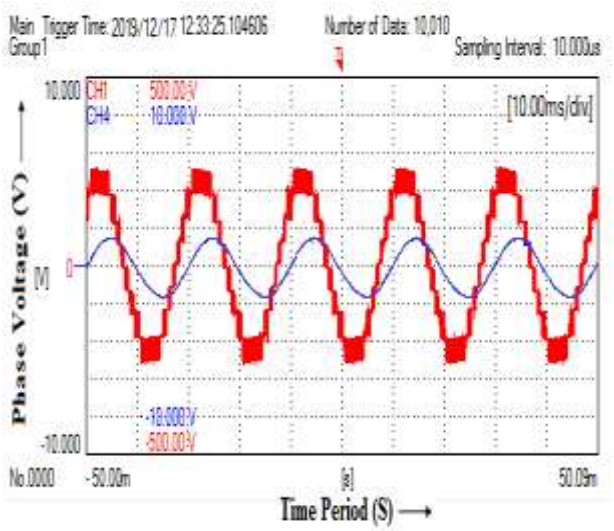


Figure 15 Waveform for Phase voltage (Va) and current (Ia) using PD ISCPWM

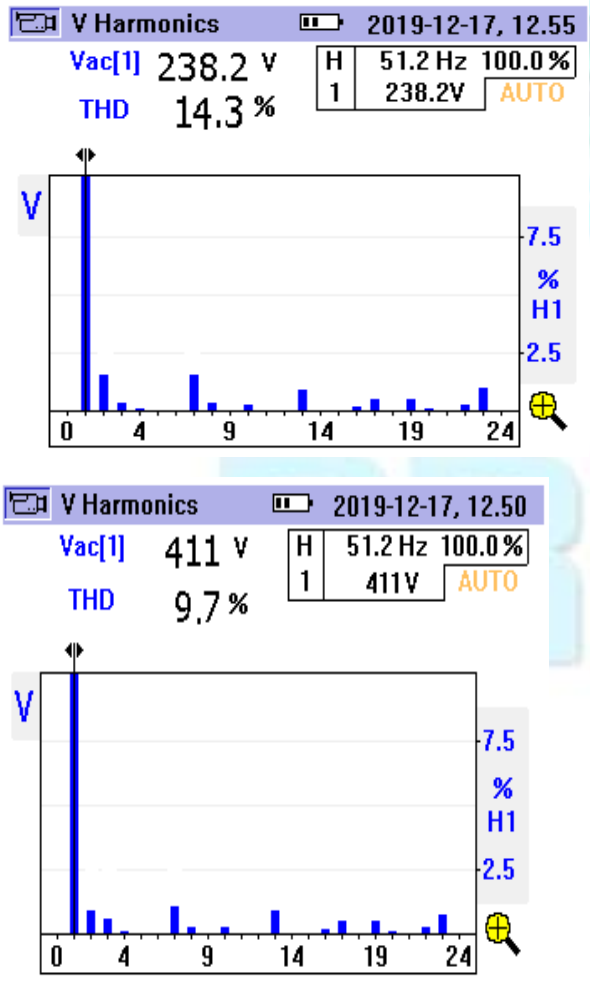


Figure 16 Spectrum using PD ISCPWM for (a) Phase voltage (Va) and (b) Line voltage ($V_{ab}$)

## CONCLUSION

A new three-phase SPSWCMLI was developed to facilitate the reduction of the switch count along the path for the current to reach various output voltage levels. The reduced switch count topology was espoused as a viable method to generate an almost sinusoidal voltage. The method of producing the PWM pulses for the switches in the MLI was based on ISCPWM approach. With a comparative analysis of the ISCPWM over the MCPWM, the simulation results were extricated to show an increase in the fundamental component of the phase voltage along with a systematic reduction of the THD levels. The experimental prototype based on FPGA was created to establish the viability of the new SPSWCMLI topology and find space in applications in the real world. The exquisite operation of the MLI will explore new areas of applications and carry the benefits of the formulation to industrial utilities.

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